Combined Impact of BTI and Temperature Effect Inversion on Circuit Performance

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***Abstract*— In the era of deep-nanoscale transistors, 3D structure of a FinFET device strengthens the self-heating effect (SHE) leading to large increase in the device temperature. Heat issues have introduced a major concern to VLSI designers since temperature is a key parameter in various aging mechanisms. This work investigates the impact of bias temperature instability (BTI) in conjunction with temperature effect inversion (TEI) on long-term circuit performance. To accurately evaluate the device aging degradation, the proposed unified TEI and BTI model considers temperature variation extracted from power dissipation in the device. The comparison of delay degradation results from our approach and other different predictions is carried out through selected combinational benchmark circuits under different operating conditions. Our approach provides highly optimistic results in which either performance degradation or improvement can be found. However, performance degradation tends to worsen at high temperature, yet lessen at high frequency.**

Keywords*—*bias temperature instability (BTI); delay degradation; FinFET; self-heating effect (SHE); temperature effect inversion (TEI)

I. INTRODUCTION

FinFETs have recently become one of the most attractive alternatives in commercial processor productions where further scaling is seriously required. However, FinFET's 3D fin-shaped structure has intensified the self-heating effect (SHE) that induces a tremendous increase in temperature due to large thermal resistance [1], [2]. Bias temperature instability (BTI) is one of the most prominent aging degradations that are strongly vulnerable to heat from SHE [3]. BTI affects both pFinFET (negative BTI or NBTI) and nFinFET (positive BTI or PBTI) causing a shift in the device threshold voltage (V_{th}). The variation in threshold voltage subsequently weakens the driving capability, worsens the delay performance, and shortens the circuit lifetime [4], [5], [6].

On the other hand, the delay characteristic of a FinFET device under temperature variation is completely different from that of its planar counterparts. As temperature rises, the temperature effect inversion (TEI) provides variation in carrier mobility and threshold voltage that alters the driving current. Under super threshold operation, TEI causes the "on" current of FinFETs to increase at high temperature [7], [8]. TEI extensively worsens the SHE due to the positive feedback loop of power dissipation and may bring the circuit into thermal runaway even at low ambient temperature. Moreover, the impact of TEI adds more difficulty to thermal management approaches because the maximum performance of each transistor is achieved at relatively high operating temperature [9].

To the best of our knowledge, this work is one of the first efforts to explore the impact of BTI on circuit performance in the presence of TEI based on power/thermal model for temperature variation. In this study, we consider that TEI and N/PBTI have a positive and negative influence, respectively, on power and delay functions. Due to this interrelation, we evaluate the convergence of temperature and all other parameters through an iterative procedure and consequently, perform long-term gate/circuit delay prediction. Under different operation scenarios, we compare the long-term delay degradation results obtained from our approaches with those from other methods. From the proposed method, most circuits under 10-year stress experience slight performance degradation (less than 2.3%), whereas some circuits gain performance improvement as much as 10%. This work provides highly optimistic results compared to the previous works.

The rest of the paper is organized as follows. Section II provides important background of thermal analysis, TEI, BTI, and some related works. The proposed simulation methodology for long-term performance prediction is introduced in section III. Experimental results and conclusion are given in sections IV and V, respectively.

II. BACKGROUND

A. *Temperature Effect Inversion*

As temperature increases, the mobility of carriers in the channel decreases due to the ionized impurity and phonon scattering [8]. While the threshold voltage in both planar and fin transistors decreases equally at high temperature, small change in the mobility of FinFET devices results in increased current. This phenomenon is called as the *temperature effect inversion* where the driving current I_{on} at all supply voltage levels is enhanced as temperature increases. The increase in driving current due to TEI improves the delay as well as raises the operating temperature in FinFET circuits. Figure 1 gives an example of the impact of TEI on driving current in a 14-nm bulk tri-gate pFinFET from [10] for different levels of V_{gs}

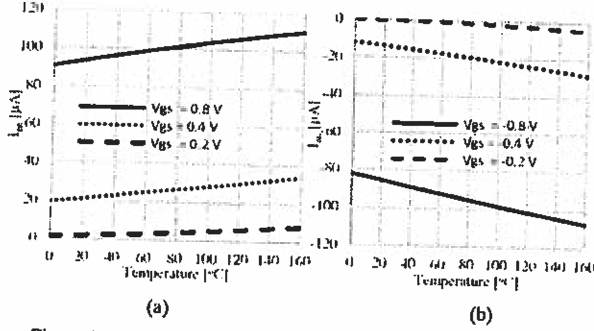

Figure 1. I_{on} under temperature variation for different V_{gs} values in the 14-nm bulk tri-gate nFinFET (a) and pFinFET (b)

according to (1) which shows I_{on} in subthreshold and superthreshold regimes [9]:

$$I_{on} = \begin{cases} \mu(T)e^{\frac{V_{gs}-V_{th}(T)}{S(T)}}, V_{gs} < V_{th} \\ \mu(T)\left(V_{gs} - V_{th}(T)\right)^{\beta}, \text{otherwise} \end{cases} \quad (1)$$

where μ, S, V_{th}, and β are the carrier mobility, the subthreshold swing, the threshold voltage, and the velocity saturation effect factor, respectively. All of these parameters are temperature- dependent

B. Temperature Modeling

The change of temperature (ΔT) from the ambient level in typical FinFETs can be modeled by evaluating the thermal resistance (R_{th}) and power dissipation (P_{dis}) under a certain operating condition as follows: [2]

$$\Delta T = R_{th}P_{dis} \quad (2)$$

The thermal resistance R_{th} is dependent on materials and geometrical structure. In particular, R_{th} of a FinFET device decreases with increasing number of fins in approximately inverse proportion [11]. The total power dissipation P_{dis} consists of two components: dynamic power P_{dyn} and static or leakage power P_{sta}; i.e., $P_{dis} = P_{dyn} + P_{sta}$. The dynamic power, which is a part of power related to switching behavior of the circuit, can be obtained from

$$P_{dyn} = \alpha C_L V_{dd}^2 f \quad (3)$$

where α is the activity factor of output node, C_L is the switching capacitance, and f is the clock frequency of the system. The activity factor α of each transistor/gate can be obtained from the input patterns. The switching capacitance C_L includes diffusion, wire, and fanout capacitance components. All the above parameters can be achieved from device level simulation. In this study, we assume that the dynamic power is unaffected by temperature variation.

The other part of power, the static power P_{sta}, has a dependence on temperature, bias voltage, and threshold voltage. P_{sta} [9], [12] can be expressed as

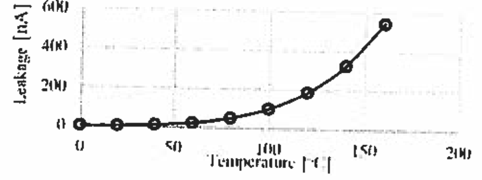

Figure 2. Leakage current under temperature variation at nominal bias condition for an inverter designed with the 14-nm bulk FinFET technology

$$P_{sta} = V_{dd}\left[c_1 T^2 e^{\left(\frac{c_2 V_{dd} + c_3 V_{th}(T)}{T}\right)} + c_4 e^{(c_5 V_{dd} + c_6)}\right] \quad (4)$$

In (4), the first term of P_{sta} is the subthreshold leakage and the last term is the gate leakage. The fitting constants, c_1 to c_6, are technology-dependent. The contribution of the gate leakage to the total leakage is insignificant compared to the subthreshold component [12]. Therefore, we assume that the gate leakage is negligible. The total leakage current varying with temperature for an inverter is illustrated in Figure 2. The exponential increase in leakage with temperature as seen in this figure adds more positive feedback to the total power dissipation inducing more heat to the circuit according to (2).

C. Bias Temperature Instability

BTI effect gradually increases the threshold voltage of a transistor over a long period of operation leading to a decrease in driving current. Both of the BTI effects can be described by the Reaction-Diffusion (RD) model. The simplified model for the long-term, worst-case threshold voltage shift $\Delta V_{th,BTI}$ covering both stress and recovery phases [3], [13], [14] can be expressed as

$$\Delta V_{th,BTI}(T, t, V_{gs}, V_{th}) = \chi\left(\frac{\sqrt{K_S^2(T, V_{gs}, V_{th}) D T_{cycle}}}{1 - K_r^{\left(\frac{1}{2n}\right)}(T, t)}\right)^{2n} \quad (5)$$

where χ is the BTI coefficient set to be 1 for NBTI and 0.5 for PBTI, K_s and K_r are fraction parameters of the stress and recovery, respectively, D is the fraction of stress time, T_{cycle} is the stress/recovery cycle time, and n is a fitting parameter set to be 1/6 for H_2-based RD model. For the same technology, the threshold voltage shift from BTI is dependent on temperature, time, bias condition, and threshold voltage.

D. Prior Work

As BTI, especially, NBTI has been considered to be a major long-term reliability concern, a number of NBTI models have been developed to address aging degradation in digital circuits during the design time. There have been many proposed techniques to predict and mitigate NBTI in SRAMs [5], [15], [16] and logic circuits [14], [17], [18], [19], [20], [21]. In [14], a closed form for the upper bound on the shift in threshold voltage ΔV_{th} is derived as a function of the duty cycle of the stress phase and clock cycle time. The work in [17] proposed a unified model for NBTI and Hot Carrier Injection (HCL) to predict threshold voltage degradation and

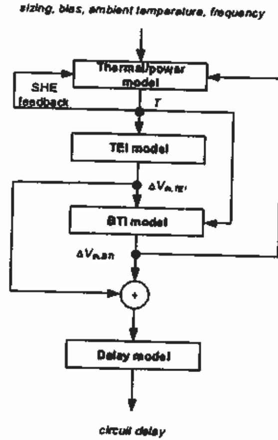

Figure 3. Block diagram for the proposed performance analysis considering TEI and BTI

circuit lifetime in various FinFET devices and small circuits. In [18], performance and reliability of standard cells are evaluated considering NBTI and process variation in future technology nodes. Self-checking sensors was developed in [19] to monitor late transition due to NBTI in critical path of combinational circuits with low area and power cost. The works in [20] and [21] primarily explored the impact of the stacking effect on NBTI degradation in planar MOSFET logic circuits. However, NBTI predictions resulted from those two works are less likely to be accurate for modern FinFET design.

Few previously proposed aging models have taken into account thermal effects in FinFET devices. In [9], a TEI-aware dynamic thermal management approach was developed to minimize energy consumption in FinFET circuits operating at the optimal temperature with no performance penalty. The work in [22] investigated the temperature dependence of leakage under NBTI stress but the TEI is not included in their evaluation. The study in [23] integrated long-term NBTI prediction with the TEI, yet the operating temperature was set to be constant for the entire circuit regardless of power dissipation consideration.

III. Simulation and Analysis Methodology

The objective of this work is to evaluate the delay degradation influenced by temperature and threshold voltage variations under TEI and BTI phenomena considering fine-grained temperature estimation from the power profile of each device. Our proposed performance/reliability simulation and analysis framework is illustrated in Figure 3 which consists of four models for temperature and power interaction, TEI, BTI, and circuit delay as will be discussed in the following subsections.

A. Thermal/Power Model

The thermal/power model gives the steady-state temperature corresponding to the power dissipation of each device. The power dissipation is derived from scratch using the fixed parameters: sizing, bias level, ambient temperature, and clock frequency, and the recursive parameters: SHE and the threshold voltage variation due to BTI. We initially consider the change in temperature in (2) as a function of the thermal resistance and dynamic/leakage power in (3) and (4), respectively. Thermal resistance can be determined using sizing information which is related to the number of fins of the FinFET device [11]. In this model, the temperature and threshold voltage feedbacks from SHE and BTI affect only the subthreshold leakage.

For dynamic power determination, logic simulation is required to know the activity factor at each output node. We firstly calculate the total dynamic power dissipation in a gate from (3). Next, we can determine the dynamic power for each transistor as follows. For each device in the parallel network, the dynamic power is distinguished by the switching activity while all devices have the same load capacitance. Therefore, the dynamic power for each parallel transistor can be obtained based on the fraction of the device switching activity. On the other hand, for each transistor in series, the dynamic power is associated with the difference in load capacitance while all stacked transistors have the same switching activity. As a result, the dynamic power for each transistor in series can be obtained based on the fraction of the device load capacitance. Because there exist feedback loops in our consideration, the convergence of temperature requires an iterative procedure. In the situation that a device falls into the thermal runaway, we also limit the dynamic power by relocating the gate fanouts to reduce the load capacitance.

B. TEI Model

In this study, we assume that the change in I_{on} under temperature variation is considered approximately equivalent to the condition that TEI induces the threshold voltage shift $\Delta V_{th,TEI}$ to the device, and hence, the carrier mobility and other temperature-dependent terms can be represented as the functions of $\Delta V_{th,TEI}$. The threshold voltage shift due to TEI $\Delta V_{th,TEI}$ that varies the driving current in (1) when the temperature changes from nominal temperature T_0 to any temperature T can now be expressed in the following equation:

$$I_{on} \cong \begin{cases} \mu(\Delta V_{th,TEI}) e^{\frac{V_{gs} - |V_{th}(T_0) + \Delta V_{th,TEI}(T)|}{S(\Delta V_{th,TEI})}}, & \textit{subthreshold regime} \\ \mu(\Delta V_{th,TEI}) [V_{gs} - [V_{th}(T_0) + \Delta V_{th,TEI}(T)]]^{\beta}, & \text{otherwise} \end{cases} \quad (6)$$

Although we can evaluate the driving current as a function of temperature, mapping the change in I_{on} to the threshold voltage shift can help simplify the problem when BTI and delay, which are threshold voltage-dependent, are involved.

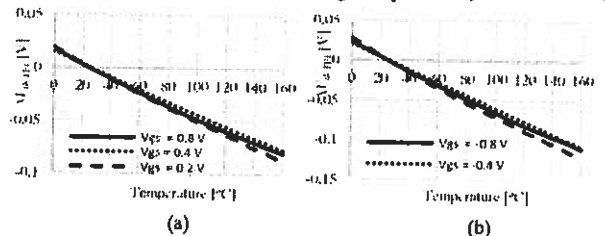

Figure 4. The equivalent shift in the threshold voltage due to TEI as a function of the target temperature in the 14-nm bulk tri-gate nFinFET (a) and pFinFET (b) for different V_{gs} values

TABLE I. 10-YEAR DELAY UNDER VARIATION IN AMBIENT TEMPERATURE

<table>
<tr><th rowspan="3">Circuit</th><th colspan="4">T_{amb} = 25 °C</th><th colspan="4">T_{amb} = 45 °C</th><th colspan="4">T_{amb} = 65 °C</th></tr>
<tr><th rowspan="2">Baseline Delay (ps)</th><th colspan="3">Delay Change due to BTI (%)</th><th rowspan="2">Baseline Delay (ps)</th><th colspan="3">Delay Change due to BTI (%)</th><th rowspan="2">Baseline Delay (ps)</th><th colspan="3">Delay Change due to BTI (%)</th></tr>
<tr><th>without $\Delta V_{th,TEI}$, Fixed T.</th><th>with $\Delta V_{th,TEI}$, Fixed T.</th><th>Proposed Approach</th><th>without $\Delta V_{th,TEI}$, Fixed T.</th><th>with $\Delta V_{th,TEI}$, Fixed T.</th><th>Proposed Approach</th><th>without $\Delta V_{th,TEI}$, Fixed T.</th><th>with $\Delta V_{th,TEI}$, Fixed T.</th><th>Proposed Approach</th></tr>
<tr><td>C499</td><td>94.39</td><td colspan="2">1.22</td><td>0.89</td><td>90.71</td><td>1.68</td><td>1.74</td><td>1.41</td><td>87.16</td><td>2.23</td><td>2.40</td><td>2.07</td></tr>
<tr><td>C880</td><td>114.75</td><td colspan="2">1.23</td><td>0.93</td><td>109.91</td><td>1.69</td><td>1.76</td><td>1.45</td><td>105.22</td><td>2.26</td><td>2.43</td><td>2.13</td></tr>
<tr><td>C1355</td><td>105.96</td><td colspan="2">1.24</td><td>0.98</td><td>101.75</td><td>1.71</td><td>1.77</td><td>1.51</td><td>97.69</td><td>2.28</td><td>2.45</td><td>2.19</td></tr>
<tr><td>C1908</td><td>140.99</td><td colspan="2">1.26</td><td>0.52</td><td>135.22</td><td>1.74</td><td>1.80</td><td>1.08</td><td>129.66</td><td>2.32</td><td>2.50</td><td>1.79</td></tr>
<tr><td>C2670</td><td>183.60</td><td colspan="2">1.16</td><td>0.47</td><td>177.10</td><td>1.58</td><td>1.64</td><td>0.97</td><td>170.91</td><td>2.08</td><td>2.24</td><td>1.60</td></tr>
<tr><td>C5315</td><td>188.66</td><td colspan="2">1.23</td><td>0.79</td><td>181.68</td><td>1.67</td><td>1.75</td><td>1.31</td><td>174.98</td><td>2.24</td><td>2.41</td><td>1.98</td></tr>
<tr><td>C6288</td><td>456.73</td><td colspan="2">1.26</td><td>1.01</td><td>438.44</td><td>1.75</td><td>1.81</td><td>1.56</td><td>420.70</td><td>2.35</td><td>2.53</td><td>2.28</td></tr>
<tr><td>C7552</td><td>157.32</td><td colspan="2">1.23</td><td>0.73</td><td>151.52</td><td>1.68</td><td>1.75</td><td>1.25</td><td>145.68</td><td>2.23</td><td>2.40</td><td>1.91</td></tr>
<tr><td>i7</td><td>221.84</td><td colspan="2">1.18</td><td>-8.43</td><td>213.98</td><td>1.61</td><td>1.67</td><td>-5.97</td><td>206.50</td><td>2.13</td><td>2.29</td><td>-3.43</td></tr>
<tr><td>i8</td><td>570.34</td><td colspan="2">1.51</td><td>-3.77</td><td>539.75</td><td>2.13</td><td>2.21</td><td>-2.79</td><td>509.86</td><td>2.90</td><td>3.13</td><td>-1.59</td></tr>
<tr><td>i9</td><td>310.73</td><td colspan="2">1.44</td><td>-9.45</td><td>297.65</td><td>2.01</td><td>2.08</td><td>-7.59</td><td>284.96</td><td>2.70</td><td>2.91</td><td>-4.56</td></tr>
<tr><td>S838</td><td>169.40</td><td colspan="2">1.04</td><td>1.02</td><td>162.78</td><td>1.44</td><td>1.49</td><td>1.46</td><td>156.39</td><td>1.91</td><td>2.06</td><td>2.02</td></tr>
<tr><td>S5378</td><td>91.67</td><td colspan="2">1.16</td><td>0.82</td><td>88.28</td><td>1.60</td><td>1.66</td><td>1.32</td><td>85.04</td><td>2.12</td><td>2.28</td><td>1.96</td></tr>
<tr><td>S15850</td><td>352.24</td><td colspan="2">1.08</td><td>0.58</td><td>339.72</td><td>1.48</td><td>1.53</td><td>1.04</td><td>327.77</td><td>1.95</td><td>2.10</td><td>1.63</td></tr>
<tr><td>S35932</td><td>191.67</td><td colspan="2">1.16</td><td>-8.74</td><td>185.25</td><td>1.58</td><td>1.64</td><td>-6.13</td><td>179.17</td><td>2.08</td><td>2.24</td><td>-3.48</td></tr>
</table>

IV. EXPERIMENTAL RESULTS

Our gate-level simulation framework is implemented in JAVA on a 2.50-GHz Intel Core i7 machine with 16-GB memory. A number of experimental circuits selected from the ISCAS-85/89 (combinational parts) and MCNC benchmark suites are mapped with the cell library that consists of Inverter, and 2- to 4-input NAND and NOR gates. All cells are designed with minimum size by the 14-nm tri-gate bulk FinFET predictive technology from [10] throughout the experiment. At normal operating condition, we set V_{dd} = 0.8 V, and the probability of input logic for all primary inputs is equally weighted. We also rearrange the fanouts of some gates when the temperature of some devices in that gate is higher than the maximum value of 125 °C.

Table I compares the delay degradation after 10 years of BTI stress in selected experimental circuits under different ambient temperatures (T_{amb}) of 25 °C, 45 °C, and 65 °C with the operating frequency of 1 GHz. All delay values are normalized with respect to the original delay before BTI degradation at each given temperature. This baseline delay varies from the nominal delay at 25 °C as a result of TEI (i.e., $\Delta V_{th,TEI} = 0$ at 25 °C). At the given ambient temperature, the change in delay estimated from three different approaches is provided. Under the delay change field, the first column contains the delay results from the conventional BTI prediction where $\Delta V_{th,TEI}$ is not included. The second column records the results from the BTI prediction proposed in [23] that takes into account $\Delta V_{th,TEI}$ at fixed temperature without thermal estimation and the feedbacks of temperature and $\Delta V_{th,BTI}$. The last column of the delay change contains the delay results from our proposed approach. Note that the positive value of % change means the circuit delay increases, whereas the negative value indicates that the circuit delay decreases from the baseline delay.

In Table I, the delay of most circuits obtained from our approach increases by 0.5 – 2.3%, yet in i7, i8, i9, and S35932, the delay decreases as much as 10%. Since we integrate power/thermal model into our evaluation, the circuits with large load capacitance (those i circuits) tend to gain the speed from heat. Further, as the ambient temperature increases, the interaction between BTI and leakage power provides more negative feedback to the TEI mechanism and hence, the degradation becomes larger for all circuits.

TABLE II. 10-YEAR DELAY DEGRADATION UNDER FREQUENCY VARIATION AT T_{AMB} = 55 °C

Circuit	Baseline Delay (ps)	10-year Delay Change (%)		
		500 MHz	1 GHz	2 GHz
C499	88.92	2.14	1.72	1.16
C880	107.54	2.17	1.77	1.25
C1355	99.71	2.22	1.83	1.33
C1908	132.42	2.04	1.41	0.46
C2670	173.97	1.84	1.27	0.40
C5315	178.29	2.10	1.63	0.96
C6288	429.50	2.29	1.90	1.41
C7552	148.71	2.06	1.56	0.84
i7	210.20	-4.00	-4.71	-5.56
i8	524.72	0.09	-2.22	NA
i9	291.26	-2.94	-6.10	-7.14
S838	159.55	1.95	1.72	1.50
S5378	86.64	2.03	1.62	1.08
S15850	333.68	1.78	1.32	0.64
S35932	182.17	-4.27	-4.81	-5.31

Compared to our work, the results from the other two methods are certainly pessimistic with substantial difference for some circuits. As temperature of all devices is assumed constant at the ambient level, these approaches yield the positive delay change (increase) from the baseline values for all experimental circuits. Because BTI degradation worsens at reduced threshold voltage, the approach that considers $\Delta V_{th,TEI}$ provides larger delay change than that from the other.

10-year delay degradation results in some selected circuits, under different operating frequencies with T_{amb} = 55 °C, are reported in Table II. The delay results in this table vary from a few percent of degradation to a moderate percent of improvement. The frequency causes a direct influence on the dynamic power, and alters the static power over the change in temperature, whereas BTI stress is slightly affected by frequency variation at beyond GHz operation. The net delay of most FinFET circuits tends to decrease at high frequency.

In this study, we consider the impact of BTI at a particular stress time. However, BTI is generally a temporal effect which also varies with time. Since taking the time dependency of BTI into consideration may add more complexity to the simulation methodology, we assume in this study that all circuits under test receive a final BTI degradation at the end of the given (10-year) operation time.

V. CONCLUSION

In this paper, we investigate the combined impact of BTI and TEI on the performance of combinational FinFET circuits. The proposed aging degradation prediction exploits the thermal/power characteristic of the device as well as the recursive effect of driving current from TEI and BTI. The results from experimental circuits designed with the 14-nm bulk tri-gate FinFET technology reveal that the 10-year circuit delay may either increase (by $0.5 - 2.3\%$) or decrease (up to 10%) under a certain power dissipation of each circuit. However, as temperature increases, BTI dominates TEI causing larger delay degradation in most circuits. On the other hand, high frequency causes stronger influence on TEI than BTI and as a result, all experimental circuits degrade slower at high frequency. We believe that this investigation may help clearly address temperature-dependent reliability issues in the future FinFET designs.

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