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# NBTI in FinFET Circuits Under the Temperature Effect Inversion

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***Abstract*—FinFET technology has increasingly been adopted for use within integrated circuits thanks to its superior electrical integrity and scalability. However, most recent studies have concluded that FinFET circuits tend to be more vulnerable to negative bias temperature instability (NBTI) compared to planar MOSFET designs as a result of the self-heating effect. In this paper, we contrarily reveal that under strong NBTI stress from increased temperature, the temperature effect inversion (TEI) in small nanometer FinFET devices significantly improves the circuit performance. From experimental results, at high temperature, the TEI impact dominates the delay degradation due to NBTI causing almost all of the experimental FinFET circuits to run faster.**

***Keywords—delay degradation; FinFET; negative bias temperature instability (NBTI); particle swarm optimization (PSO); temperature effect inversion (TEI)***

## I. Introduction

In deep nanometer regime, while conventional planar MOSFET devices are increasingly vulnerable to reliability degradation, Fin-Field Effect Transistors or FinFETs become one of the most favorable alternative structures providing higher robustness against reliability deterioration and potentially enabling further scaling. The FinFET exhibits several advantages over the planar transistor, especially in decreased leakage power and better electrical integrity [1], [2], [3] with minor modifications to traditional manufacturing processes [4], [5]. Moreover, FinFET circuits have stronger soft error immunity and receive less effect of process variation on their performance [6]. Although the FinFET can solve many reliability issues found in its planar counterparts, some recent studies have revealed that the lifetime of FinFET circuits tends to be shorter than that of conventional MOSFET designs as a result of the *negative bias temperature instability (NBTI)* [3], [7], [8]. NBTI is a temporal mechanism that causes a shift in threshold voltage ($V_{th}$) in a P-channel device when its gate-source voltage ($V_{gs}$) is negative. The shift in threshold voltage subsequently influences long-term reliability of a circuit such as weaker driving capability, poorer delay performance, and shorter circuit lifetime. Since FinFET geometrical structure is non-planar, the sidewall interface between gate oxide and conducting channel expands Si-H bond availability, thereby accelerating threshold voltage degradation in the device [9]. On the other hand, fin structure of each transistor also raises the self-heating effect as a result of large thermal resistance causing the increase in operating temperature, the key factor that worsens NBTI degradation [10]. The continuous increase in transistor density from technology scaling also makes heat issues more difficult to manage. However, heat may not lead to an immense increase in the circuit delay due to NBTI in the state-of-the-art technology as reported in this paper.

It has been described in [11], [12], and [13] that the delay of circuits designed with below 20-nm FinFET technologies decreases as temperature increases in both subthreshold and super threshold operations. Unlike the delay of the planar devices which normally worsens at higher temperature under super threshold voltage operation, a large amount of heat in FinFET circuits can help improve the circuit performance. This contrary behavior against that we have found in conventional MOSFETs is called as the *temperature effect inversion (TEI)* phenomenon. The TEI that causes the worst delay performance to happen at the lowest chip temperature brings different concerns in thermal management for modern processors.

To the best of our knowledge, this work is one of the first efforts that take into consideration the TEI phenomenon for NBTI simulation and analysis in FinFET circuits. In our proposed NBTI simulation, we use the particle swarm optimization (PSO) algorithm [14] to construct an accurate TEI-aware long-term threshold voltage shift model from cycle-by-cycle NBTI degradation history by means of solving a nonlinear fitting problem since this evolutionary algorithm is easy to implement and fast to converge. The delay degradation is then evaluated with regard to the increase and decrease in threshold voltage due to NBTI and TEI, respectively. From the experimental results, most benchmark circuits operating under NBTI stress for up to 10 years can even receive performance improvement at high temperature.

The rest of the paper is organized as follows. Section II provides important background of NBTI and TEI phenomena. Some other related works are discussed in section III. The proposed TEI-aware long-term NBTI estimation is introduced in section IV. Sections V and VI give experimental results and conclusion, respectively.

## II. Background

### A. Dynamic NBTI Model

NBTI effect can be described by the Reaction-Diffusion (R-D) theory [15], [16]. The reaction starts at the $Si/SiO_2$

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interface of a negatively biased P-channel transistor. There are some broken Si-H bonds at the interface as a result of holes from the inversion layer tunneling into the gate oxide. This reaction (or the so-called "stress phase") generates incomplete $Si^{+}$ bonds at the interface (interface traps) and releases H atoms diffusing away from the interface. When the negative bias is removed, some of the hydrogen species diffuse back and repassivate the broken $Si^{+}$ bonds. The dynamic model for threshold voltage shift ($\Delta V_{th}$) covering both stress and recovery phases can be obtained [1] from the following equations:

$$\text{Stress: } \Delta V_{th}(t) = \left[K_v(t-t_0)^{\frac{1}{2}} + \sqrt[2n]{\Delta V_{th}(t_0)}\right]^{2n} \quad (1)$$

$$\text{Recovery: } \Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{2t_{ox}+\sqrt{Ct}}\right) \quad (2)$$

where $C$ is the diffusion temperature-dependent coefficient; $n$ is set to be 1/4 or 1/6 for H diffusion or $H_2$ diffusion, respectively [17]; the times $t_0$ and $t_1$ correspond to the time at the beginning of stress phase and recovery phase, respectively; $\xi_1$ and $\xi_2$ are back diffusion constants; $t_e$ is the effective diffusion distance; $t_{ox}$ is the oxide thickness; and the term $K_v$ is given by

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K_1^{\,2} C_{ox}(V_{gs} - V_{th0})\sqrt{C}exp\left(\frac{2E_{ox}}{E_0}\right) \quad (3)$$

where $E_{ox}$ is the vertical electric field, $E_0$ is a technology dependent parameter, $K_1$ is a constant, $V_{gs}$ is the gate-source voltage of the device, and $V_{th0}$ is the original threshold voltage.

### B. Temperature Effect Inversion (TEI)

Generally, the mobility of carriers in the channel decreases at high temperature due to the ionized impurity and phonon scatterings which are temperature-dependent [12]. The decrease in carrier mobility in planar MOSFETs is larger compared to that in FinFETs since heavily doped body is required to reduce the short-channel effect. On the other hand, undoped body in FinFETs causes lower mobility degradation. As temperature increases, threshold voltage in both devices

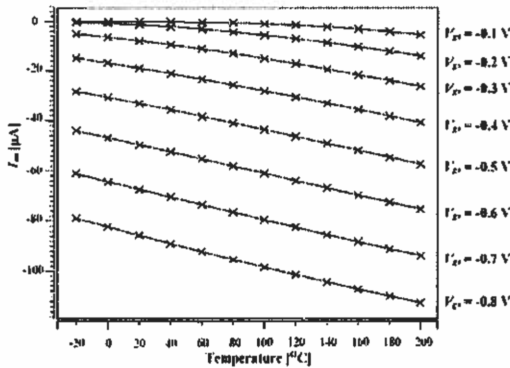

Figure 1. $I_{on}$ under temperature variation for different $V_{gs}$ values in the 14-nm bulk tri-gate PFinFET

decreases moderately while the mobility in FinFET devices slightly degrades. These effects result in the net change in the driving current ($I_{on}$) according to the following equation [13].

$$I_{on} = \begin{cases} \mu(T)e^{\frac{V_{gs}-V_{th}(T)}{S(T)}}, V_{gs} < V_{th} \\ \mu(T)\left(V_{gs} - V_{th}(T)\right)^{\beta}, \text{otherwise} \end{cases} \quad (4)$$

where $\mu$, $S$, $V_{th}$, and $\beta$ are the carrier mobility, the subthreshold swing, the threshold voltage, and the velocity saturation effect factor, respectively. All of these parameters are temperature-dependent.

This behavior of the driving current in FinFET devices as discussed above is called as the *temperature effect inversion* where $I_{on}$ at all supply voltage levels is enhanced as temperature increases. An example of the TEI phenomenon in a PFinFET is illustrated in Figure 1 which shows the temperature dependence of $I_{on}$ in the 14-nm bulk tri-gate PFinFET from [18] for different levels of $V_{gs}$. This increase in $I_{on}$ can be considered equivalent to the reduction in threshold voltage that results in performance improvement.

## III. Related Work

A number of NBTI models have been developed to address aging degradation in digital circuits during the design time. For FinFET based SRAMs, some techniques have lately been proposed to predict NBTI as well as to improve SRAM reliability against NBTI [1], [2], [8]. There have also been other recent efforts to investigate NBTI degradation in logic circuits as follows. The work in [19] described a unified model for both NBTI and Hot Carrier Injection (HCL) to predict threshold voltage degradation and circuit lifetime in various FinFET devices and small circuits. The work in [5] modeled the performance and reliability of standard cells considering NBTI and process variation in future technology nodes. The delay effects and frequency dependence of NBTI in high-k/metal gate FinFET logic circuits was investigated in [20]. Analysis of NBTI in datapath logic subblocks at netlist level in [21] reveals that the correlation of NBTI aging sensitivity to workload variations and architectural parameters is remarkably high. In [16], a closed form for the upper bound on $\Delta V_{th}$ is derived as a function of the duty cycle of the stress phase and clock cycle time. The works in [22] and [23] primarily explored the impact of the stacking effect on NBTI degradation in planar MOSFET logic circuits. However, NBTI predictions resulted from these two works are less likely to be accurate for modern FinFET designs.

Few previously proposed NBTI models have taken into account thermal effects in FinFET devices. The work in [24] described an NBTI/leakage analysis and optimization framework considering the temperature variation which is close to our consideration but the TEI is not included in their NBTI evaluation. Reference [13] describes a TEI-aware dynamic thermal management approach to minimize energy consumption in FinFET circuits operating at the optimal temperature with no performance penalty. However, to the

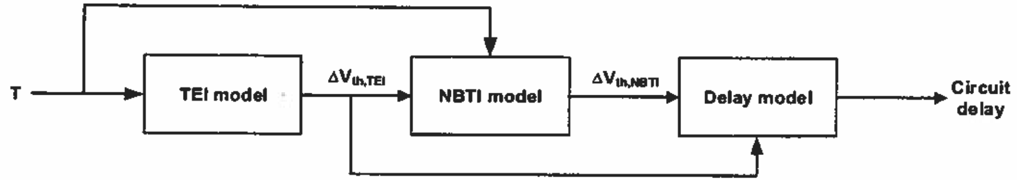


Figure 2. Interrelation among the reliability and performance models

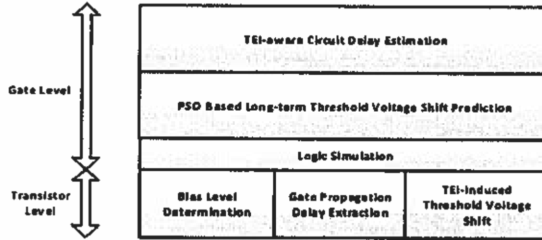


Figure 3. TEI-aware NBTI simulation framework

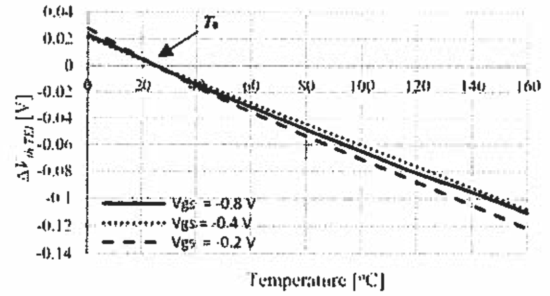


Figure 4. The equivalent shift in the threshold voltage due to TEI as a function of the target temperature in the 14-nm bulk tri-gate PFinFET for different $V_{gs}$ values

best of our knowledge, none of aging models has correlated the influence of TEI and thus, aging reliability results predicted by those recently proposed approaches are rather pessimistic.

## IV. SIMULATION METHODOLODY

In this study, we introduce a novel NBTI degradation model coupled with the TEI which is a unique characteristic of the FinFET devices. The diagram illustrating the interrelation among TEI, NBTI, and delay effects considered in our work is given in Figure 2. At a particular operating temperature, the TEI model maps temperature of all devices into the threshold voltage shift due to TEI ($\Delta V_{th,TEI}$) which is firstly introduced by this work. This variation also affects the NBTI mechanism resulting in the other threshold voltage shift ( $\Delta V_{th,NBTI}$ ). Typically, $\Delta V_{th,TEI}$ is negative, whereas $\Delta V_{th,NBTI}$ is positive. These two opposite outcomes, in turn, change the delay of the device and circuit.

The framework shown in Figure 3 covers hierarchical NBTI modeling from the transistor level to gate level of the design. At the transistor level, we perform extensive SPICE simulation to obtain bias voltage and propagation delay profiles as well as TEI-induced threshold voltage shift under temperature variation for all gates in our design library. Logic simulation is performed to obtain the input-dependent property of the bias voltage level that is further used to construct the long-term threshold voltage shift model. Afterwards, as a function of the node capacitance and the net threshold voltage shift due to both NBTI and TEI, the circuit delay can be determined. Finally, we apply the proposed NBTI model to a number of experimental FinFET circuits to explore the long-term circuit delay degradation in the presence of TEI.

### A. TEI model

In this study, the change in $I_{on}$ under temperature variation is considered approximately equivalent to the condition that the TEI induces the threshold voltage shift $\Delta V_{th,TEI}$ to a device. Particularly, this equivalent threshold voltage shift introduced in our work reasonably encapsulates the two effects of mobility and threshold voltage changes that bring the driving current from $I_{on}$ at nominal temperature $T_0$ to $I_{on}$ at any temperature $T$. Now, all temperature-dependent terms of the driving current in (4) are represented as the functions of $\Delta V_{th,TEI}$ as follows.

$$I_{on} \cong \begin{cases} \mu(\Delta V_{th,TEI}) e^{\frac{V_{gs}-[V_{th}(T_0)+\Delta V_{th,TEI}(T)]}{s(\Delta V_{th,TEI})}}, subthreshold\ regime \\ \mu(\Delta V_{th,TEI})[V_{gs} - [V_{th}(T_0) + \Delta V_{th,TEI}(T)]]^{\beta}, \text{otherwise} \end{cases} \quad (5)$$

The proposed TEI model in (5) requires SPICE simulation to map the change in temperature into the equivalent threshold voltage shift $\Delta V_{th,TEI}$. The relationship between temperature and $\Delta V_{th,TEI}$ is given in Figure 4. In this figure, $\Delta V_{th,TEI}$ of the 14-nm bulk tri-gate PFinFET from [18] for some $V_{gs}$ levels is plotted with the target temperature $T$ at which we need to identify the corresponding $I_{on}$. It can be further noticed in this figure that the reduction of $\Delta V_{th,TEI}$ is almost constant as temperature increases for wide range of the bias levels. As seen in Figure 4, we can reasonably assume that $\Delta V_{th,TEI}$ is independent on $V_{gs}$ for all supply voltage levels. The equivalent threshold voltage shift due to TEI $\Delta V_{th,TEI}$, defined in this work, can simply be included in some performance/reliability functions that rely on the threshold voltage such as NBTI and delay. For example, to integrate the

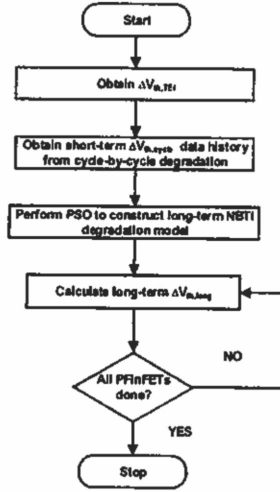


Figure 5. Flowchart of PSO based TEI-aware long-term NBTI prediction

TEI into the NBTI model in (3), we add $\Delta V_{th,TEI}$ into the original threshold voltage; i.e., $V_{th0} \leftarrow V_{th0} + \Delta V_{th,TEI}$. Generally, $\Delta V_{th,TEI}$ of the FinFET is negative when the temperature increases. This worsens the NBTI stress in (1), yet at the same time, causes the circuit delay to decrease.

### *B. NBTI model*

In this work, PSO algorithm is used to construct a long-term NBTI model guided by the dynamic degradation in (1), (2), and (3). PSO is one of the evolutionary computation methods to search for potential solutions based on swarm intelligence of insects, birds, or fish. In PSO, an individual or particle is represented by its position and velocity which indicate a possible solution and search direction, respectively. All particles iteratively evaluate their move and update the position and velocity based on their own and group's (swarm's) experiences. The position and velocity vectors of the $i$-th particle in the $d$-dimensional search space are represented as $\mathbf{P}_i = [p_{i,1}, p_{i,2}, p_{i,3},\ldots, p_{i,d}]^T$ and $\mathbf{V}_i = [v_{i,1}, v_{i,2}, v_{i,3},\ldots, v_{i,d}]^T$, respectively. Each particle has its own personal best position, $\mathbf{P}_i^b = [p_{i,1}^b, p_{i,2}^b, p_{i,3}^b,\ldots, p_{i,d}^b]^T$, achieved at the end of $j$-iteration. In the entire swarm, the best of the personal best position found so far is represented as the global best position, $\mathbf{P}^g = [p_1^g, p_2^g, p_3^g,\ldots, p_d^g]^T$. At the ($j$+1)-iteration, the particle velocity, $\mathbf{V}_i^{j+1}$, and position, $\mathbf{P}_i^{j+1}$, are updated according to the evolution equations [25] as follows.

$$\mathbf{V}_i^{j+1} = \omega*\mathbf{V}_i^j + c_1*r_1*(\mathbf{P}^g - \mathbf{P}_i^j) + c_2*r_2*(\mathbf{P}_i^b - \mathbf{P}_i^j) \quad (6)$$

$$\mathbf{P}_i^{j+1} = \mathbf{P}_i^j + \mathbf{V}_i^j \quad (7)$$

In (6) and (7), $\omega$ is the inertia weight, $c_1$ and $c_2$ are the learning factors, and $r_1$ and $r_2$ are random numbers in [0, 1].

Flowchart of our proposed PSO based long-term NBTI prediction is shown in Figure 5. Since a PFinFET receives arbitrary stress level and time duration, depending on its $V_{gs}$ for each input cycle, the results from the dynamic model are recorded as degradation history that helps capture stress-recovery pattern of the device under actual operation. The long-term NBTI degradation at the time $t$ in a PFinFET can be approximated as the power law degradation:

$$\Delta V_{th,long}(t) = K_c * t^{K_e} \quad (8)$$

where $K_c$ and $K_e$ are constants which are dependent on various operating parameters such as the supply voltage, temperature, probability of stress, input cycle time, and device geometrical parameters.

A nonlinear problem is formulated to fit the input-dependent constants, $K_c$ and $K_e$, in (8). The objective is to minimize the sum of square error (*SSE*) between the short-term cycle-by-cycle data ($\Delta V_{th,cycle}$) resulted from (1) and (2) and the generated long-term degradation data ($\Delta V_{th,long}$) in (8). The *SSE* can be described as

$$SSE = \sum_{k=1}^{\#of\ data\ points} [\Delta V_{th,cycle}(t_k) - \Delta V_{th,long}(t_k)]^2 \quad (9)$$

In summary, the nonlinear fitting problem used for constructing the long-term threshold voltage degradation model due to NBTI can be stated as

**Fit:** $K_c, K_e$

**Min:** *SSE* (10)

Next, we employ PSO to solve the above nonlinear problem. In this study, the generated values for each particle $i$, $K_{c,i}$ and $K_{e,i}$, associated with the fitting constants, $K_c$

```
//Initialization
for each particle i = 1 to swarm size do {
      Randomly generate Pi and Vi
      Pi^b ← Pi
      Save SSE of each Pi^b
}// end for each particle

Save minimum SSE of the swarm
P^g  ← best {Pi^b, i = 1,...,swarm size}//Pi^b with minimum SSE

//Main Loop
for each iteration j = 1 to #of max iteration do {

      //Evaluation
      for each particle i = 1 to swarm size do {
            if (SSE of Pi < SSE of Pi^b) then {
                  Pi^b ← Pi
                  Save SSE of current Pi^b
            }
            if (SSE of Pi^b < SSE of P^g) then {
                  P^g ← Pi^b
                  Save minimum SSE
            }
      }// end for each particle

      //Update
      for each particle i = 1 to swarm size do {
            Vi ← ω*Vi + c1*r1*(P^g − Pi) + c2*r2* (Pi^b − Pi)
            Pi ← Pi + Vi
            // ω is the inertia weight
            // c1 and c2 are the learning factors
            // r1 and r2 are random numbers in [0, 1]

      }//end for each particle

}//end for each iteration
```

Figure 6. Pseudocode of PSO algorithm for long-term NBTI prediction

TABLE I. MAXIMUM THRESHOLD VOLTAGE DEGRADATION IN EACH MAPPING GATE BY THE END OF $10^4$-S STRESS WITH $10^3$-HZ INPUT FREQUENCY AND 125 °C OPERATING TEMPERATURE

| Gate | Maximum $\Delta V_{th}$ | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $M_0$ | | | $M_1$ | | | $M_2$ | | | $M_3$ | | |
| | Cycle-by-cycle(mV) | Long-term(mV) | % Difference | Cycle-by-cycle(mV) | Long-term(mV) | % Difference | Cycle-by-cycle(mV) | Long-term(mV) | % Difference | Cycle-by-cycle(mV) | Long-term(mV) | % Difference |
| INV | 48.61 | 49.83 | 2.51 | - | - | - | - | - | - | - | - | - |
| NOR2 | 48.61 | 49.83 | 2.51 | 42.01 | 42.91 | 2.14 | - | - | - | - | - | - |
| NOR3 | 48.61 | 49.83 | 2.51 | 44.52 | 46.11 | 3.57 | 39.39 | 40.24 | 2.16 | - | - | - |
| NOR4 | 48.61 | 49.83 | 2.51 | 46.91 | 49.02 | 4.50 | 43.14 | 44.22 | 2.50 | 28.50 | 29.00 | 1.72 |

and $K_e$, are described as the position of a 2-dimensional particle ($d = 2$), and thus, $\mathbf{P}_i = [K_{c,i}, K_{e,i}]^T$. Figure 6 sketches the pseudocode of PSO algorithm applied to this problem. To begin with, the position and velocity vectors, $\mathbf{P}_i$ and $\mathbf{V}_i$, are initialized with random values. Because there is no previous $\mathbf{P}_i$ value for comparison in this initialization stage, the personal best position of the $i$-th particle, $\mathbf{P}_i^b$, is set to be the same as $\mathbf{P}_i$. In the main loop of PSO algorithm, the current particle position, $\mathbf{P}_i$, is evaluated and compared with the previous personal best position, $\mathbf{P}_i^b$, and the global best position, $\mathbf{P}^g$. If the current $\mathbf{P}_i$ provides smaller *SSE*, it will replace $\mathbf{P}_i^b$ or both $\mathbf{P}_i^b$ and $\mathbf{P}^g$. At the end of the main loop, the particle velocity, $\mathbf{V}_i$, and position, $\mathbf{P}_i$, are updated according to the evolution equations [25], and set to be the velocity and position of the corresponding particle for the next iteration.

The results from the PSO based threshold voltage shift in the basic logic gates are verified with those from the cycle-by-cycle based approaches under $10^4$-second stress as reported in Table I. In cycle-by-cycle based NBTI prediction, equally weighted 1-kHz inputs are provided to each gate under 125 °C operating temperature and hence, this approach requires $10^7$ cycles to complete the task. Note that the threshold voltage shift in Table I is the change in the threshold voltage at 125 °C as a result of NBTI (TEI is also involved). We performed the proposed long-term PSO based NBTI prediction with 20 particles, 100 iterations, and 200 to 1000 data points (cycles) from the cycle-by-cycle based data. For all gates, PFinFET $M_0$ is connected to the power supply followed by $M_1$, $M_2$, and $M_3$. Table I shows that the proposed PSO based NBTI model yields satisfactory results bounded within 4.5% of the referenced cycle-by-cycle based model.

## C. Propagation Delay Model

Our proposed propagation delay model evaluates the circuit performance under TEI and NBTI. As the net threshold voltage shift (summation of $\Delta V_{th,TEI}$ and $\Delta V_{th,NBTI}$) considered in this work is input-dependent, each FinFET in a gate receives different levels of the total threshold voltage shift. Estimating the circuit timing performance requires a propagation delay model that can cope with this unequal threshold voltage degradation among pull-up transistors. Further, since this study mainly focuses on the impact of NBTI on PFinFETs, the term "delay" used in the rest of this paper is indeed the "rise time propagation delay".

We modify the delay model from [22] to calculate the delay in FinFET circuits as a function of the threshold voltage shift and the gate fanouts, defining the load capacitance. First of all, we assume that all PFinFETs have original threshold

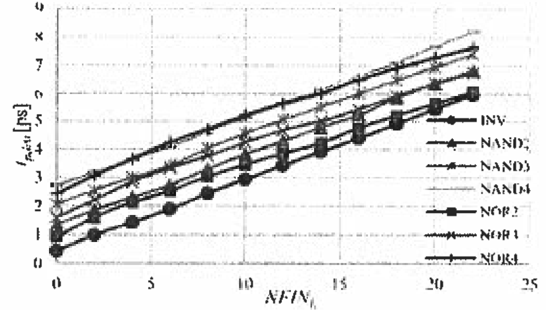


Figure 7. Original rising propagation delay for different load capacitance

voltage of $v_{tp0}$ and rising propagation delay of $t_{pdr0}$ which has a linear relationship with the load capacitance. Since in this work, the size of both PFinFET and NFinFET with one fin and single finger is assumed identical, the load capacitance can be reasonably considered linear with the total number of fins ($NFIN_L$) of PFinFETs and NFinFETs connected to the output of the gate. Hence, if all devices have the same number of fingers, we can consider that $t_{pdr0}$ has linear relation with $NFIN_L$ as given below.

$$t_{pdr0} = A\, NFIN_L + B \tag{11}$$

where $NFIN_L$ is the total number of fins of the gate fanouts. The constants, $A$ and $B$, depend on the gate type and can be identified by linear fitting. Figure 7 plots $t_{pdr0}$ of various gates versus $NFIN_L$ when their load is an inverter with varying size. In this figure, we can see the nearly linear relationship between $t_{pdr0}$ and $NFIN_L$. These plots are used to fit all constants in (11) for all of the gates in the design library.

For a series of PFinFETs, suppose that $t_{pdr0,i}$ is a component of original delay corresponding to PFinFET $M_i$ where $t_{pdr0} = \sum_i t_{pdr0,i}$. For small change in the threshold voltage of PFinFET $M_i$ from $v_{tp0}$ to $v_{tp0} + \Delta v_{tp,i}$ that causes the component of original delay corresponding to PFinFET $M_i$ to change from $t_{pdr0,i}$ to $t_{pdr0,i} + \Delta t_{pdr,i}$, an approximate form of the Elmore delay [22], [26] can be expressed as

$$\Delta t_{pdr,i} = \frac{\alpha \Delta v_{tp,i}}{v_{dd} - v_{tp0}} t_{pdr0,i} \tag{12}$$

where $\Delta t_{pdr,i}$ is the change in the rising propagation delay component corresponding to PFinFET $M_i$ as a result of the

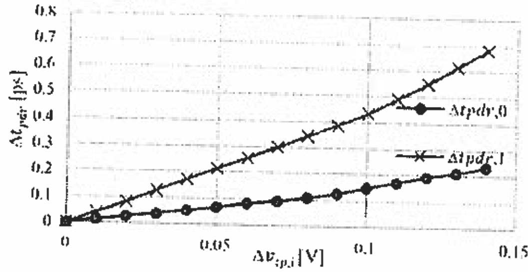


Figure 8. Changes in rising propagation delay in a 2-input NOR gate as a result of threshold voltage shift in each PFinFET

total shift in threshold voltage $\Delta v_{tp,i}$ for this device. The $\Delta v_{tp,i}$ value includes the threshold voltage shift from both TEI and NBTI; i.e., $\Delta v_{tp,i} = \Delta V_{th,long} + \Delta V_{th,TEI}$.

For Inverter and NAND cases, the maximum change in rising propagation delay, $\Delta t_{pdr,max}$, takes place when only one parallel PFinFET with the largest threshold voltage degradation, $\Delta v_{tp,max}$, turns on. It can be noticed from the relationship in (12) that $\Delta t_{pdr,i}$ is proportional to $\Delta v_{tp,i}$; i.e., for an Inverter or NAND gate,

$$\Delta t_{pdr,max} = C_1 \cdot t_{pdr0} \cdot \Delta v_{tp,max} \tag{13}$$

where $t_{pdr0}$ can be obtained from (11) and the proportional constant $C_1$ of each gate can be identified by the linear relationship at any fixed value of load capacitance.

For a NOR gate, the degradation of each PFinFET in series involves in the total $\Delta t_{pdr}$ of the gate. In this case, we assume that the component $t_{pdr0,i}$ also has the linear relationship with the intrinsic and load capacitance corresponding to PFinFET $M_i$ in series as expressed in the following equation.

$$t_{pdr0,i} = a_i\, NFIN_L + b_i \tag{14}$$

where $a_i$ and $b_i$ are parameters of the changes in load capacitance and intrinsic capacitance, respectively. For any NOR gate, $\sum a_i = A$ and $\sum b_i = B$, where $A$ and $B$ are previously defined in (11). Together with (12) and (14), the change in rising propagation delay of the NOR gate as a result of the shift in threshold voltage in PFinFET $M_i$ can be obtained from the following equation.

$$\Delta t_{pdr,i} = C_2 \cdot (a_i\, NFIN_L + b_i) \cdot \Delta v_{tp,i} \tag{15}$$

where the gate constant $C_2$ and transistor constants, $a_i$ and $b_i$, can be identified by the linear relationship between $\Delta v_{tp,i}$ and $\Delta t_{pdr,i}$ under no load ( $NFIN_L = 0$) and under a fixed value of load capacitance. Figure 8 shows the changes in rising propagation delay of a 2-input NOR gate with $NFIN_L$ = 8 when each of the PFinFET $M_0$ and PFinFET $M_1$ receives threshold voltage degradation (but not at the same time) and causes the changes in rising delay, $\Delta\ t_{pdr,0}$ and $\Delta\ t_{pdr,1}$, respectively. It can be seen that the plots in Figure 8 underscore the linear expression in (15) for small amount of threshold voltage shift.

TABLE II. PROPAGATION DELAY MODEL VERIFICATION

| Gate | $t_{pdr}$ (ps) (SPICE) | $t_{pdr}$ (ps) (proposed model) | % Difference |
|---|---|---|---|
| | | $NFIN_L = 6$ | |
| INV | 2.0891 | 2.1213 | 0.58 |
| NAND2 | 2.9955 | 3.0190 | 0.78 |
| NAND3 | 3.8194 | 3.9224 | 2.70 |
| NAND4 | 4.5212 | 4.6646 | 3.17 |
| NOR2 | 2.7832 | 2.7211 | -2.23 |
| NOR3 | 3.5693 | 3.6159 | 1.31 |
| NOR4 | 4.5687 | 4.5793 | 0.23 |
| | | $NFIN_L = 8$ | |
| INV | 2.6708 | 2.6708 | -1.05 |
| NAND2 | 3.6317 | 3.6735 | 1.15 |
| NAND3 | 4.4332 | 4.4708 | 0.85 |
| NAND4 | 5.1068 | 5.2282 | 2.38 |
| NOR2 | 3.2702 | 3.2224 | -1.46 |
| NOR3 | 4.1442 | 4.1367 | -0.18 |
| NOR4 | 5.0459 | 5.0992 | 1.06 |

Since the total rising propagation delay of a gate, $t_{pdr}$, is equal to the original rising propagation delay added by the change due to threshold voltage degradation, the rising propagation delay can be stated as

$$t_{pdr} = t_{pdr0} + \begin{cases} \sum_{i=0}^{\#ofinputs-1} \Delta t_{pdr,i}, for\ NORs \\ \Delta t_{pdr,max}, for\ NANDs/INVs \end{cases} \tag{16}$$

To verify the propagation delay model, we compare the rising propagation delay in some basic logic gates resulted from SPICE and our model as given in Table II. In this experiment, the output of a gate is connected to an Inverter with different size ($NFIN_L$ = 6 and 8) and each PFinFET in the gate has threshold voltage shift as reported in the first column of each $M_i$ in Table I. The experimental results in Table II demonstrate that our proposed delay model provides accurate outcome with few percent difference varying from 0.2% to 3.2% with respect to the referenced model.

As discussed in this and the previous sections, although the TEI can strengthen the NBTI stress resulting in larger $\Delta V_{th,long}$, $\Delta V_{th,TEI}$ which is more negative at higher temperature directly moderates the impact of NBTI on the circuit delay. We will explore how these two phenomena influence the net delay of a number of large experimental circuits in the next section.

## V. EXPERIMENTAL RESULTS

This section gives experimental results and discusses some interesting remarks found in the study. Our gate-level simulation framework was implemented in JAVA on a 2.50-GHz Intel Core i7 machine with 16-GB memory. A number of experimental circuits selected from the ISCAS-85/89 (combinational parts) and MCNC suites were mapped with the cell library that consists of Inverter, and 2- to 4-input NAND and NOR gates. We used the14-nm tri-gate bulk FinFET predictive technology from [18] throughout the experiment. At normal operating condition, we set $V_{dd}$ = 0.8 V, and the probability of input logic for all primary inputs was equally weighted.

TABLE III. 10-YEAR DELAY UNDER TEMPERATURE VARIATION

| Circuit | Baseline Delay at 25 °C [ps] | Normalized Delay | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | *35 °C* | | | *75 °C* | | | *125 °C* | | |
| | | *TEI* | *NBTI without TEI* | *NBTI with TEI* | *TEI* | *NBTI without TEI* | *NBTI with TEI* | *TEI* | *NBTI without TEI* | *NBTI with TEI* |
| C17 | 10.626 | 0.9860 | 1.0198 | 1.0061 | 0.9263 | 1.0338 | 0.9629 | 0.8413 | 1.0567 | 0.9087 |
| C499 | 85.410 | 0.9866 | 1.0183 | 1.0052 | 0.9292 | 1.0313 | 0.9632 | 0.8477 | 1.0524 | 0.9100 |
| C880 | 100.699 | 0.9864 | 1.0180 | 1.0047 | 0.9283 | 1.0308 | 0.9617 | 0.8458 | 1.0515 | 0.9070 |
| C1196 | 69.510 | 0.9865 | 1.0182 | 1.0050 | 0.9291 | 1.0310 | 0.9627 | 0.8489 | 1.0519 | 0.9092 |
| C1355 | 97.217 | 0.9863 | 1.0189 | 1.0055 | 0.9277 | 1.0322 | 0.9626 | 0.8444 | 1.0540 | 0.9086 |
| C1908 | 119.086 | 0.9867 | 1.0180 | 1.0049 | 0.9298 | 1.0307 | 0.9631 | 0.8490 | 1.0514 | 0.9101 |
| C2670 | 191.638 | 0.9878 | 1.0170 | 1.0051 | 0.9357 | 1.0292 | 0.9672 | 0.8616 | 1.0492 | 0.9194 |
| C5315 | 171.653 | 0.9871 | 1.0182 | 1.0056 | 0.9321 | 1.0310 | 0.9658 | 0.8540 | 1.0520 | 0.9157 |
| C6288 | 378.969 | 0.9865 | 1.0191 | 1.0059 | 0.9291 | 1.0326 | 0.9644 | 0.8473 | 1.0546 | 0.9122 |
| C7552 | 142.340 | 0.9872 | 1.0180 | 1.0055 | 0.9324 | 1.0308 | 0.9658 | 0.8546 | 1.0516 | 0.9158 |
| i5 | 18.197 | 0.9859 | 1.0201 | 1.0064 | 0.9259 | 1.0343 | 0.9631 | 0.8405 | 1.0575 | 0.9087 |
| i6 | 202.643 | 0.9885 | 1.0165 | 1.0053 | 0.9396 | 1.0281 | 0.9700 | 0.8700 | 1.0471 | 0.9259 |
| i7 | 173.813 | 0.9880 | 1.0169 | 1.0052 | 0.9370 | 1.0288 | 0.9683 | 0.8645 | 1.0483 | 0.9219 |
| i8 | 425.042 | 0.9848 | 1.0204 | 1.0055 | 0.9198 | 1.0348 | 0.9575 | 0.8274 | 1.0583 | 0.8967 |
| i9 | 235.703 | 0.9856 | 1.0212 | 1.0071 | 0.9242 | 1.0361 | 0.9633 | 0.8368 | 1.0605 | 0.9087 |
| S838 | 151.903 | 0.9866 | 1.0156 | 1.0024 | 0.9293 | 1.0266 | 0.9580 | 0.8476 | 1.0445 | 0.9005 |
| S5378 | 77.501 | 0.9869 | 1.0172 | 1.0045 | 0.9313 | 1.0294 | 0.9631 | 0.8521 | 1.0493 | 0.9106 |
| S13207 | 236.662 | 0.9877 | 1.0135 | 1.0014 | 0.9350 | 1.0231 | 0.9601 | 0.8602 | 1.0387 | 0.9062 |
| S15850 | 307.890 | 0.9877 | 1.0159 | 1.0038 | 0.9352 | 1.0271 | 0.9646 | 0.8606 | 1.0453 | 0.9145 |
| S35932 | 154.566 | 0.9886 | 1.0164 | 1.0052 | 0.9400 | 1.0279 | 0.9702 | 0.8709 | 1.0468 | 0.9264 |
| AVERAGE | | 0.9869 | 1.0209 | 1.0050 | 0.9308 | 1.0305 | 0.9639 | 0.8513 | 1.0511 | 0.9118 |

Table III records the circuit delay after 10 years of NBTI stress in the experimental circuits under different temperature levels of 35 °C, 75 °C, and 125 °C with different TEI and NBTI analysis scenarios. All delay values are normalized with respect to the baseline delay at 25 °C in the second column of the table. For each temperature, in the first column which contains the normalized delay of the circuits under TEI regardless of aging degradation, it can be seen that the TEI can enhance the delay of all experimental circuits as temperature increases. Under TEI, the delay decreases by 1.3%, 7%, and 15% on average at 35 °C, 75 °C, and 125 °C, respectively. On the other hand, the second column of each temperature, which lists the normalized delay of the circuits under NBTI without TEI consideration, shows that the NBTI worsens the circuit delay as temperature increases. However, the rate of delay degradation due to NBTI with respect to the increase in temperature is relatively small compared to the delay improvement by the TEI. For example, the largest delay degradation under NBTI stress regardless of TEI is around 6% in the circuit i9 whereas the TEI can improve the performance of this circuit by 16%. The impact of the TEI tends to dominate NBTI effect at high temperature for all of the experimental circuits causing the net delay to decrease.

Under the NBTI stress coupled with the TEI (see the last column of each temperature in Table III), the circuit performance at low temperature slightly degrades due to the domination of the NBTI over the TEI. At 35 °C, the combined effects of NBTI and TEI cause the average delay to increase by 0.5%. On the contrary, at the high temperature of 125 °C, the delay decreases as much as 10% in some circuits under these two phenomena. If we consider the impact of NBTI on the circuits under TEI at a particular temperature by comparing the first and last columns of each temperature in Table III, it can also be noticed that the circuit delay due to NBTI increasingly worsens at high temperature. In the experiment, the performance degraded from the baseline delay at 35 °C, 75 °C, and 125 °C (the first column of each temperature) are 1.8%, 3.5%, and 7.1%, respectively.

In this study, the operating temperature is assumed to be constant for each analysis. However, during actual operation, the temperature of a part of the circuit dynamically changes upon the power dissipation, workload patterns, and thermal resistance. A more accurate NBTI prediction requires increasingly complicated thermal/power models to identify the steady-state temperature which affects the degradation and timing performance for different parts of the circuit. Furthermore, future work directions extended from this investigation may include an exploration of other temperature-dependent aging mechanisms that are more severely vulnerable to heat than NBTI.

## VI. CONCLUSION

In this paper, we introduce a simulation and analysis framework to address the combined impacts of NBTI and TEI on combinational circuits designed with the 14-nm bulk tri-gate FinFET technology. In the proposed framework, we develop a long-term threshold voltage shift prediction that comprehensively takes into account the TEI coupled with NBTI by using the PSO algorithm. In conjunction with the delay estimation, the results of the net delay for various large benchmark circuits show that the average delay of all circuit decreases as temperature rises due to the domination of the TEI over the NBTI. We believe that the outcomes of this investigation will lead to a right direction for improving temperature-dependent reliability degradation in the future processor design.

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interface of a negatively biased P-channel transistor. There are some broken Si-H bonds at the interface as a result of holes from the inversion layer tunneling into the gate oxide. This reaction (or the so-called "stress phase") generates incomplete $Si^{+}$ bonds at the interface (interface traps) and releases H atoms diffusing away from the interface. When the negative bias is removed, some of the hydrogen species diffuse back and repassivate the broken $Si^{+}$ bonds. The dynamic model for threshold voltage shift ($\Delta V_{th}$) covering both stress and recovery phases can be obtained [1] from the following equations:

$$\text{Stress: } \Delta V_{th}(t) = \left[K_v(t-t_0)^{\frac{1}{2}} + \sqrt[2n]{\Delta V_{th}(t_0)}\right]^{2n} \quad (1)$$

$$\text{Recovery: } \Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{2t_{ox}+\sqrt{Ct}}\right) \quad (2)$$

where $C$ is the diffusion temperature-dependent coefficient; $n$ is set to be 1/4 or 1/6 for H diffusion or $H_2$ diffusion, respectively [17]; the times $t_0$ and $t_1$ correspond to the time at the beginning of stress phase and recovery phase, respectively; $\xi_1$ and $\xi_2$ are back diffusion constants; $t_e$ is the effective diffusion distance; $t_{ox}$ is the oxide thickness; and the term $K_v$ is given by

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K_1{}^2 C_{ox}(V_{gs} - V_{tho})\sqrt{C}exp\left(\frac{2E_{ox}}{E_0}\right) \quad (3)$$

where $E_{ox}$ is the vertical electric field, $E_0$ is a technology dependent parameter, $K_1$ is a constant, $V_{gs}$ is the gate-source voltage of the device, and $V_{tho}$ is the original threshold voltage.

### *B. Temperature Effect Inversion (TEI)*

Generally, the mobility of carriers in the channel decreases at high temperature due to the ionized impurity and phonon scatterings which are temperature-dependent [12]. The decrease in carrier mobility in planar MOSFETs is larger compared to that in FinFETs since heavily doped body is required to reduce the short-channel effect. On the other hand, undoped body in FinFETs causes lower mobility degradation. As temperature increases, threshold voltage in both devices

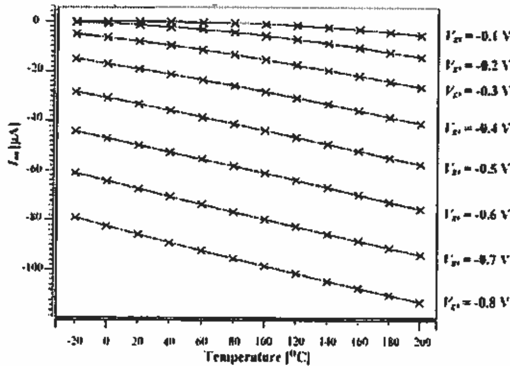


Figure 1. $I_{on}$ under temperature variation for different $V_{gs}$ values in the 14-nm bulk tri-gate PFinFET

decreases moderately while the mobility in FinFET devices slightly degrades. These effects result in the net change in the driving current ($I_{on}$) according to the following equation [13].

$$I_{on} = \begin{cases} \mu(T)e^{\frac{V_{gs}-V_{th}(T)}{S(T)}}, V_{gs} < V_{th} \\ \mu(T)\left(V_{gs} - V_{th}(T)\right)^{\beta}, \text{otherwise} \end{cases} \quad (4)$$

where $\mu$, $S$, $V_{th}$, and $\beta$ are the carrier mobility, the subthreshold swing, the threshold voltage, and the velocity saturation effect factor, respectively. All of these parameters are temperature-dependent.

This behavior of the driving current in FinFET devices as discussed above is called as the *temperature effect inversion* where $I_{on}$ at all supply voltage levels is enhanced as temperature increases. An example of the TEI phenomenon in a PFinFET is illustrated in Figure 1 which shows the temperature dependence of $I_{on}$ in the 14-nm bulk tri-gate PFinFET from [18] for different levels of $V_{gs}$. This increase in $I_{on}$ can be considered equivalent to the reduction in threshold voltage that results in performance improvement.

## III. RELATED WORK

A number of NBTI models have been developed to address aging degradation in digital circuits during the design time. For FinFET based SRAMs, some techniques have lately been proposed to predict NBTI as well as to improve SRAM reliability against NBTI [1], [2], [8]. There have also been other recent efforts to investigate NBTI degradation in logic circuits as follows. The work in [19] described a unified model for both NBTI and Hot Carrier Injection (HCL) to predict threshold voltage degradation and circuit lifetime in various FinFET devices and small circuits. The work in [5] modeled the performance and reliability of standard cells considering NBTI and process variation in future technology nodes. The delay effects and frequency dependence of NBTI in high-k/metal gate FinFET logic circuits was investigated in [20]. Analysis of NBTI in datapath logic subblocks at netlist level in [21] reveals that the correlation of NBTI aging sensitivity to workload variations and architectural parameters is remarkably high. In [16], a closed form for the upper bound on $\Delta V_{th}$ is derived as a function of the duty cycle of the stress phase and clock cycle time. The works in [22] and [23] primarily explored the impact of the stacking effect on NBTI degradation in planar MOSFET logic circuits. However, NBTI predictions resulted from these two works are less likely to be accurate for modern FinFET designs.

Few previously proposed NBTI models have taken into account thermal effects in FinFET devices. The work in [24] described an NBTI/leakage analysis and optimization framework considering the temperature variation which is close to our consideration but the TEI is not included in their NBTI evaluation. Reference [13] describes a TEI-aware dynamic thermal management approach to minimize energy consumption in FinFET circuits operating at the optimal temperature with no performance penalty. However, to the